sufficiently small when the FET is in the OFF state, and the variable ratio of the amount of signal transmission can be improved.

REMARKS

Favorable reconsideration of this application as presently amended is respectfully requested.

Claims 1-20 are active in this application; Claims 1 and 11 having been amended by way of the present Amendment.

In the outstanding Official Action, Claims 1-20 were rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention; Claims 1-10 were rejected under 35 USC §103(a) as being unpatentable over Fisher; Claims 11, 13, 14, 16, 17, 18 and 20 were rejected under 35 USC §103(a) as being unpatentable over Bohan, Jr.; and Claims 12, 15 and 19 were objected to as being dependent upon a rejected base claims, but were otherwise indicated as being allowable if rewritten in independent form.

Applicants acknowledge with appreciation the indication that Claims 12, 15 and 19 include allowable subject matter. However, since Applicants consider that amended Claims 1 and 11 are allowable, Claims 12, 15 and 19 have presently been maintained in dependent form.

The above changes to the specification and Abstract correct minor informalities and are not believed to raise a question of new matter

In response to the outstanding rejection under 35 USC §112, second paragraph, Claims 1 and 11 have been amended to clarify that the series resonance circuit is formed of the reactance component of the gate-to-source impedance and the

inductor element when the drain voltage of the FET is lower than the source voltage thereof, and that an inductance value of the inductor element is set in accordance with a frequency of said controlled signal. In view of these changes to Claims 1 and 11, the claims are believed to be definite and the outstanding rejection under 35 USC §112, second paragraph, is believed to have been overcome. If, however, the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work with the Examiner in a joint effort to derive mutually satisfactory claim language.

Turning now to the several grounds for rejection on the merits, Applicants point out that with the provision of a series resonance circuit formed of the reactance component of the gate-to-source impedance and the inductor element when the drain voltage of the FET is lower than the source voltage thereof, and with the inductance value of the inductor element set in accordance with the frequency of the controlled signal as claimed, it is possible to substantially bring the resonance frequency of the above-mentioned series resonance circuit into line with the frequency of the controlled signal. Therefore, it is possible to reduce the amount of transmitting the signal when the FET is in the OFF state.

In regard to the rejection of claims 1-10 as obvious over the Fisher patent, Applicants acknowledge that Fisher in Fig. 1 shows an oscillation circuit having an inductor connected between the source terminal of the FET 12 and the ground terminal. In the circuit of Fisher, however, no controlled signal is inputted to the gate terminal of the FET 12, and no signal corresponding to the controlled signal is outputted from the drain terminal of the FET 12. Furthermore, there is no disclosure in Fisher that the inductor is part of a series resonance circuit, nor is there disclosure in Fisher that the inductance value of the inductor element is set in accordance with

the frequency of a controlled signal as claimed. In view of these deficiencies in Fisher, it is respectfully submitted that Fisher in no way obviates the claimed invention and that Claims 1-10 patentably define over Fisher.

As recited in claims 11-20, the series resonance circuit is formed of the reactance component of the gate-to-source impedance and the inductor element, and the inductance value of the inductor element is set in accordance with the frequency of the controlled signal. Therefore, it is possible to sufficiently reduce the amount of transmitting the signal when the FET is in the OFF state, thereby reducing the power consumption of the semiconductor integrated circuit.

In contrast, the applied Bohan patent discloses an oscillator means 20 in which is provided an FET 21, and an inductor 28 and capacitor 26 connected in series between the source terminal of the FET 21 and the ground terminal. Although Bohan discloses the provision of the oscillator means 20, Bohan fails to disclose or suggest that the Bohan inductor constitutes a portion of a series resonance circuit and fails to disclose provision of the claimed series resonance circuit. Furthermore, as with the Fisher patent, Bohan fails further to disclose or suggest that the inductance value of the inductor element is set in accordance with the frequency of the controlled signal, which failure is readily evident insofar as no controlled signal is inputted to the oscillator means 20 of Bohan. Thus, it cannot be said that the inductance value of the inductor 28 of Bohan is set in accordance with the frequency of a controlled signal, as claimed. For these reasons, it is respectfully submitted that claims 11-20 patentably distinguish over Bohan.

Consequently, in view of the present amendment and in light of the above comments, the pending claims are believed to be in condition for allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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IN THE SPECIFICATION

Please amend the paragraphs in the specification identified below as shown in clean form below. A marked-up copy of amended paragraphs is attached.

Page 1, lines 27-30, please amend this paragraph as follows:

FIG. 1 is an equivalent circuit diagram of an FET. Using this equivalent circuit, the reason why the amount of signal transmission cannot sufficiently be lowered when the FET is in the OFF state will be described below.

Page 2, lines 20-24, please amend this paragraph as follows:

It is therefore an object of the present invention to eliminate the

10, so that it is possible to sufficiently decrease the amount of signal transmission when the FET 10 is in the OFF state.

IN THE CLAIMS:

Please amend claims 1 and 11 as follows.

1. (Amended) A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal and a drain terminal configured to output a signal corresponding to said controlled signal; and

an inductor element provided between a source terminal and a ground terminal of said FET,

wherein [an inductance value of said inductor element is set so that said inductor element resonates in series for a reactance component of a gate-to-source impedance by said controlled signal] when a drain voltage of said FET is lower than a source voltage thereof, a series resonance circuit it formed of a reactance component of a gate-to-source impedance and said inductor element, and an inductance value of said inductor element is adjusted in accordance with a frequency of said controlled signal.

11. (Amended) A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal and a drain terminal configured to output a signal corresponding to said controlled signal; and

an inductor element and a first capacitor element which are connected to each other in series between a source terminal and a ground terminal of said FET,

wherein [an inductance value of said inductor element is set so that said inductor element resonates in series for a reactance component of agate-to-source impedance by said controlled signal] when a drain voltage of said FET is lower than a source voltage thereof, a series resonance circuit is formed of a reactance component of a gate-to-source impedance and said inductor element, and an inductance value of

said inductor element is adjusted in accordance with a frequency of said controlled signal.

IN THE ABSTRACT

Please amend page 17, lines 2-21:

[It is an object of the present invention to provide a] A semiconductor integrated circuit capable of decreasing the amount of signal transmission when an FET is in an OFF state and of improving a variable ratio of the amount of signal transmission[.], including [The semiconductor integrated circuit according to the present invention comprises:] an inductor element provided between the source terminal and ground terminal of an FET; and Lo input matching circuit provided between the gate terminal and input terminal of the FET; a bias supply circuit connected to the gate terminal of the FET; an RF output matching circuit provided between the drain terminal and output terminal of the FET; a control signal input circuit connected to the drain terminal of the FET; and a bias supply circuit connected to the source terminal of the FET. Since the reactance component of the gate-to-source impedance of the FET series-resonates with the inductor element 1 when the FET is in the OFF state, the amount of signal transmission can be sufficiently small when the FET is in the OFF state, and the variable ratio of the amount of signal transmission can be improved.